

# High Voltage High Side/ Low Side N-Channel MOSFET Driver

## FEATURES

- Bootstrap Supply Voltage Up to 114V
- Wide  $V_{CC}$  Voltage: 7.2V to 13.5V
- 2.5A Peak Top Gate Pull-Up Current
- 3A Peak Bottom Gate Pull-Up Current
- $1.2\Omega$  Top Gate Driver Pull-Down
- $0.55\Omega$  Bottom Gate Driver Pull-Down
- 5ns Top Gate Fall Time Driving 1nF Load
- 8ns Top Gate Rise Time Driving 1nF Load
- 3ns Bottom Gate Fall Time Driving 1nF Load
- 6ns Bottom Gate Rise Time Driving 1nF Load
- Drives Both High and Low Side N-Channel MOSFETs
- Undervoltage Lockout
- Thermally Enhanced 8-Pin MSOP Package

## APPLICATIONS

- Distributed Power Architectures
- Automotive Power Supplies
- High Density Power Modules
- Telecommunication Systems

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## DESCRIPTION

The LTC<sup>®</sup>4446 is a high frequency high voltage gate driver that drives two N-channel MOSFETs in a DC/DC converter with supply voltages up to 100V. The powerful driver capability reduces switching losses in MOSFETs with high gate capacitance. The LTC4446's pull-up for the top gate driver has a peak output current of 2.5A and its pull-down has an output impedance of  $1.2\Omega$ . The pull-up for the bottom gate driver has a peak output current of 3A and the pull-down has an output impedance of  $0.55\Omega$ .

The LTC4446 is configured for two supply-independent inputs. The high side input logic signal is internally level-shifted to the bootstrapped supply, which may function at up to 114V above ground.

The LTC4446 contains undervoltage lockout circuits that disable the external MOSFETs when activated.

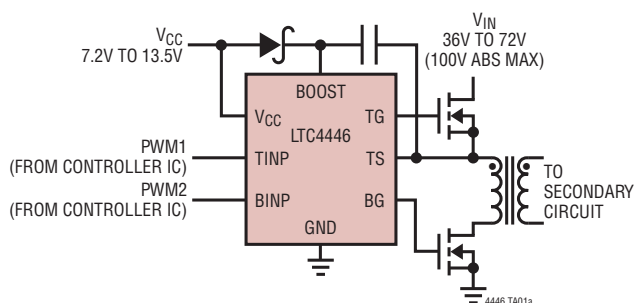
The LTC4446 is available in the thermally enhanced 8-lead MSOP package.

The LTC4446 does not have adaptive shoot-through protection. For similar drivers with adaptive shoot-through protection, please refer to the chart below.

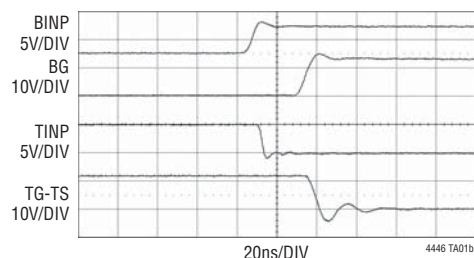
PARAMETER	LTC4446	LTC4444	LTC4444-5
Shoot-Through Protection	No	Yes	Yes
Absolute Max TS	100V	100V	100V
MOSFET Gate Drive	7.2V to 13.5V	7.2V to 13.5V	4.5V to 13.5V
$V_{CC}$ UV <sup>+</sup>	6.6V	6.6V	4V
$V_{CC}$ UV <sup>-</sup>	6.15V	6.15V	3.55V

## TYPICAL APPLICATION

Two Switch Forward Converter



LTC4446 Driving a 1000pF Capacitive Load



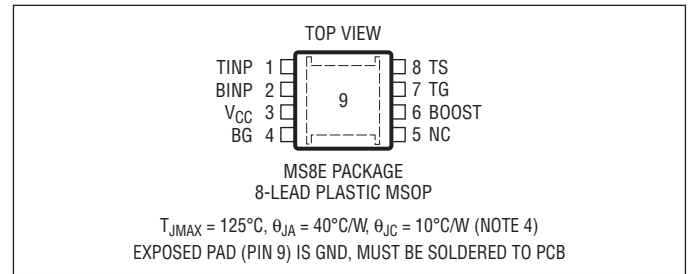
## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage

$V_{CC}$ .....	-0.3V to 14V
BOOST – TS.....	-0.3V to 14V
TINP Voltage.....	-2V to 14V
BINP Voltage.....	-2V to 14V
BOOST Voltage.....	-0.3V to 114V
TS Voltage.....	-5V to 100V
Operating Temperature Range (Note 2)....	-40°C to 85°C
Junction Temperature (Note 3).....	125°C
Storage Temperature Range.....	-65°C to 150°C
Lead Temperature (Soldering, 10 sec).....	300°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4446EMS8E#PBF	LTC4446EMS8E#TRPBF	LTDPZ	8-Lead Plastic MSOP	-40°C to 85°C
LTC4446IMS8E#PBF	LTC4446IMS8E#TRPBF	LTDPZ	8-Lead Plastic MSOP	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = V_{BOOST} = 12\text{V}$ ,  $V_{TS} = \text{GND} = 0\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Gate Driver Supply, <math>V_{CC}</math></b>							
$V_{CC}$	Operating Voltage		7.2		13.5	V	
$I_{VCC}$	DC Supply Current	TINP = BINP = 0V		350	550	$\mu\text{A}$	
UVLO	Undervoltage Lockout Threshold	$V_{CC}$ Rising	●	6.00	6.60	7.20	V
		$V_{CC}$ Falling Hysteresis	●	5.60	6.15	6.70	V mV
<b>Bootstrapped Supply (BOOST – TS)</b>							
$I_{BOOST}$	DC Supply Current	TINP = BINP = 0V		0.1	2	$\mu\text{A}$	
<b>Input Signal (TINP, BINP)</b>							
$V_{IH(BG)}$	BG Turn-On Input Threshold	BINP Ramping High	●	2.25	2.75	3.25	V
$V_{IL(BG)}$	BG Turn-Off Input Threshold	BINP Ramping Low	●	1.85	2.3	2.75	V
$V_{IH(TG)}$	TG Turn-On Input Threshold	TINP Ramping High	●	2.25	2.75	3.25	V
$V_{IL(TG)}$	TG Turn-Off Input Threshold	TINP Ramping Low	●	1.85	2.3	2.75	V
$I_{TINP(BINP)}$	Input Pin Bias Current			$\pm 0.01$	$\pm 2$	$\mu\text{A}$	
<b>High Side Gate Driver Output (TG)</b>							
$V_{OH(TG)}$	TG High Output Voltage	$I_{TG} = -10\text{mA}$ , $V_{OH(TG)} = V_{BOOST} - V_{TG}$		0.7		V	
$V_{OL(TG)}$	TG Low Output Voltage	$I_{TG} = 100\text{mA}$ , $V_{OL(TG)} = V_{TG} - V_{TS}$	●	120	220	mV	
$I_{PU(TG)}$	TG Peak Pull-Up Current		●	1.7	2.5	A	
$R_{DS(TG)}$	TG Pull-Down Resistance		●	1.2	2.2	$\Omega$	

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = V_{\text{BOOST}} = 12\text{V}$ ,  $V_{TS} = \text{GND} = 0\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Low Side Gate Driver Output (BG)</b>						
$V_{\text{OH(BG)}}$	BG High Output Voltage	$I_{\text{BG}} = -10\text{mA}$ , $V_{\text{OH(BG)}} = V_{\text{CC}} - V_{\text{BG}}$		0.7		V
$V_{\text{OL(BG)}}$	BG Low Output Voltage	$I_{\text{BG}} = 100\text{mA}$	●	55	110	mV
$I_{\text{PU(BG)}}$	BG Peak Pull-Up Current		●	2	3	A
$R_{\text{DS(BG)}}$	BG Pull-Down Resistance		●	0.55	1.1	$\Omega$
<b>Switching Time (BINP (TINP) is Tied to Ground While TINP (BINP) is Switching. Refer to Timing Diagram)</b>						
$t_{\text{PLH(TG)}}$	TG Low-High (Turn-On) Propagation Delay		●	25	45	ns
$t_{\text{PHL(TG)}}$	TG High-Low (Turn-Off) Propagation Delay		●	22	40	ns
$t_{\text{PLH(BG)}}$	BG Low-High (Turn-On) Propagation Delay		●	19	35	ns
$t_{\text{PHL(BG)}}$	BG High-Low (Turn-Off) Propagation Delay		●	14	30	ns
$t_{\text{DM(BGTG)}}$	Delay Matching BG Turn-Off and TG Turn-On		●	-15	10	ns
$t_{\text{DM(TGBG)}}$	Delay Matching TG Turn-Off and BG Turn-On		●	-25	-3	ns
$t_{\text{r(TG)}}$	TG Output Rise Time	10% – 90%, $C_L = 1\text{nF}$ 10% – 90%, $C_L = 10\text{nF}$		8 80		ns ns
$t_{\text{f(TG)}}$	TG Output Fall Time	10% – 90%, $C_L = 1\text{nF}$ 10% – 90%, $C_L = 10\text{nF}$		5 50		ns ns
$t_{\text{r(BG)}}$	BG Output Rise Time	10% – 90%, $C_L = 1\text{nF}$ 10% – 90%, $C_L = 10\text{nF}$		6 60		ns ns
$t_{\text{f(BG)}}$	BG Output Fall Time	10% – 90%, $C_L = 1\text{nF}$ 10% – 90%, $C_L = 10\text{nF}$		3 30		ns ns

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC4446E is guaranteed to meet specifications from  $0^\circ\text{C}$  to  $85^\circ\text{C}$ . Specifications over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operating temperature range are assured by design, characterization and correlation

with statistical process controls. The LTC4446I is guaranteed over the full  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operating temperature range.

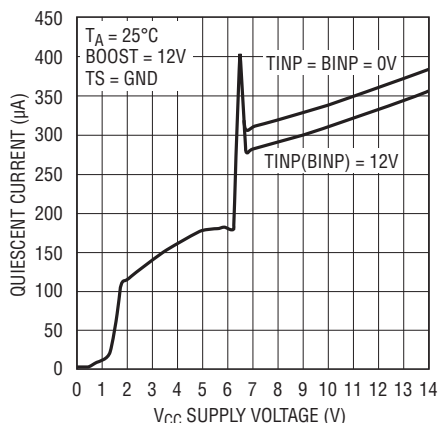
**Note 3:**  $T_J$  is calculated from the ambient temperature  $T_A$  and power dissipation  $P_D$  according to the following formula:

$$T_J = T_A + (P_D \cdot \theta_{JA} \text{ } ^\circ\text{C/W})$$

**Note 4:** Failure to solder the exposed back side of the MS8E package to the PC board will result in a thermal resistance much higher than  $40^\circ\text{C/W}$ .

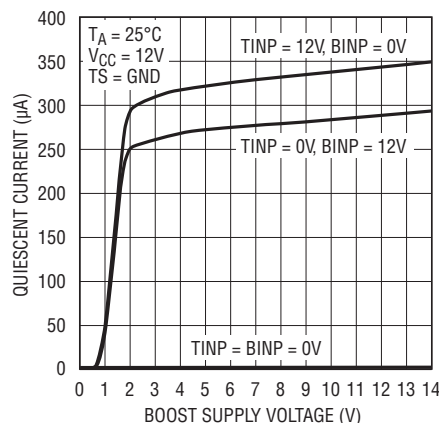
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$  Supply Quiescent Current vs Voltage**



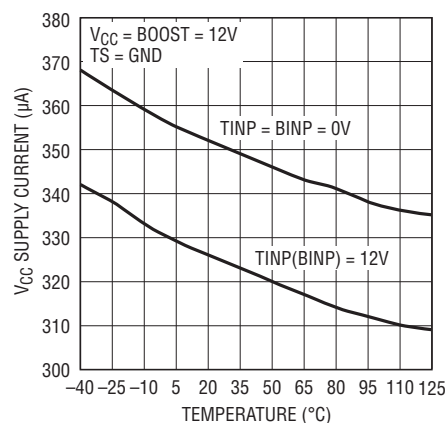
4446 G01

**BOOST-TS Supply Quiescent Current vs Voltage**



4446 G02

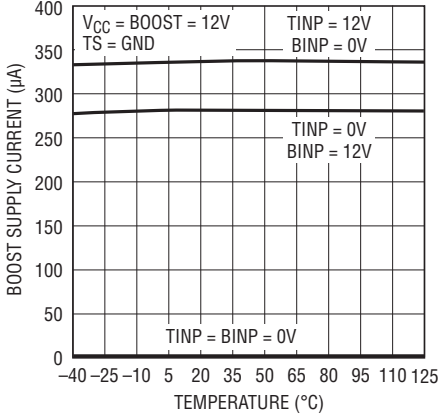
**$V_{CC}$  Supply Current vs Temperature**



4446 G03

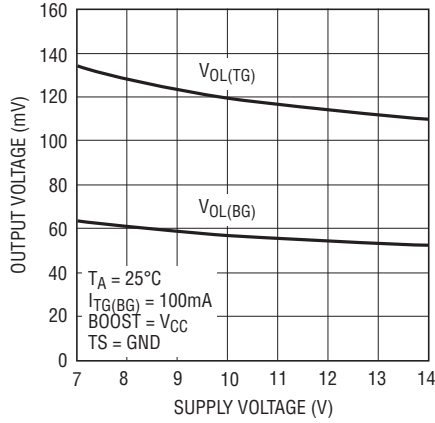
## TYPICAL PERFORMANCE CHARACTERISTICS

**Boost Supply Current vs Temperature**



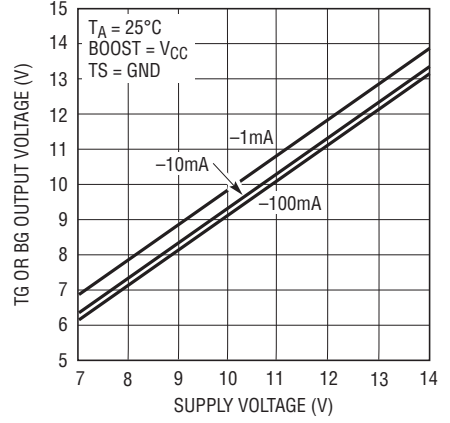
4446 G04

**Output Low Voltage ( $V_{OL}$ ) vs Supply Voltage**



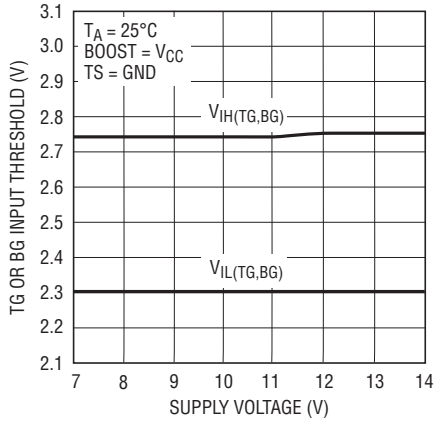
4446 G05

**Output High Voltage ( $V_{OH}$ ) vs Supply Voltage**



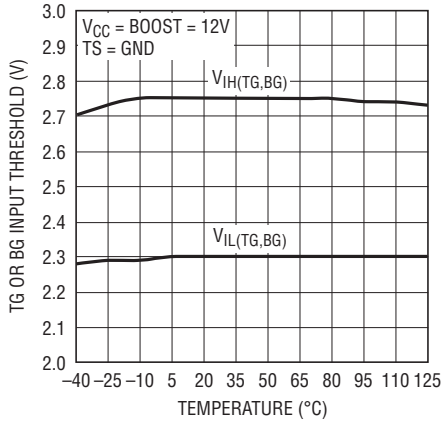
4446 G06

**Input Thresholds ( $T_{INP}$ ,  $B_{INP}$ ) vs Supply Voltage**



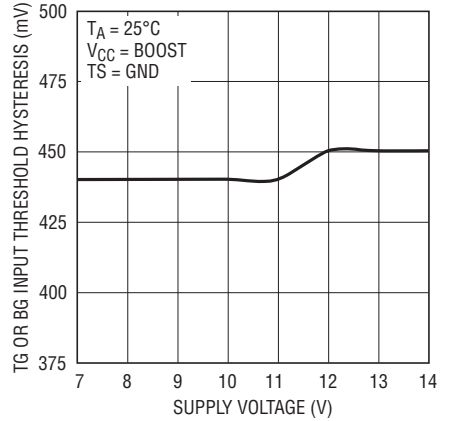
4446 G07

**Input Thresholds ( $T_{INP}$ ,  $B_{INP}$ ) vs Temperature**



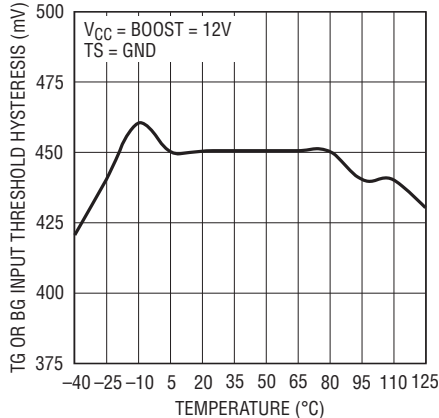
4446 G08

**Input Thresholds ( $T_{INP}$ ,  $B_{INP}$ ) Hysteresis vs Voltage**



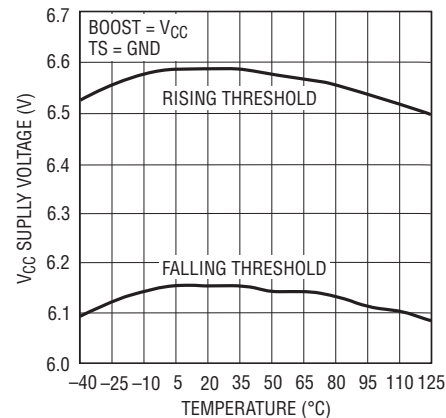
4446 G09

**Input Thresholds ( $T_{INP}$ ,  $B_{INP}$ ) Hysteresis vs Temperature**



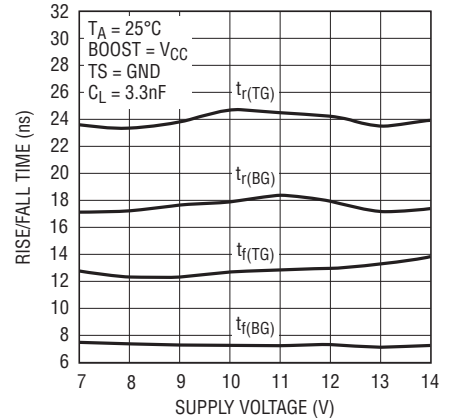
4446 G10

**$V_{CC}$  Undervoltage Lockout Thresholds vs Temperature**



4446 G11

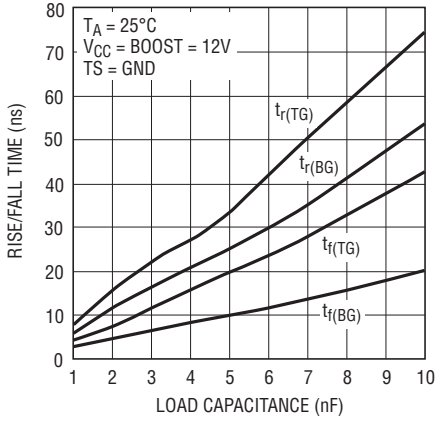
**Rise and Fall Time vs  $V_{CC}$  Supply Voltage**



4446 G12

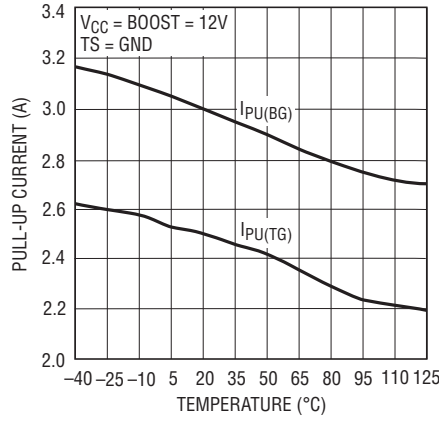
# TYPICAL PERFORMANCE CHARACTERISTICS

**Rise and Fall Time vs Load Capacitance**



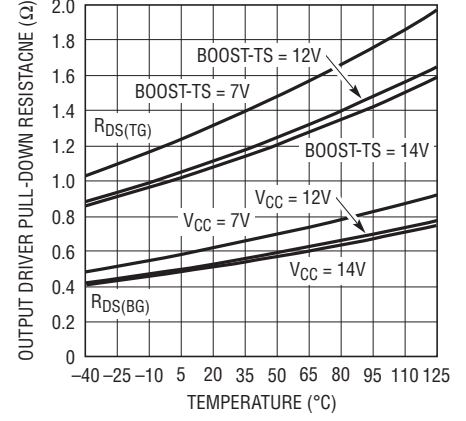
4445 G13

**Peak Driver (TG, BG) Pull-Up Current vs Temperature**



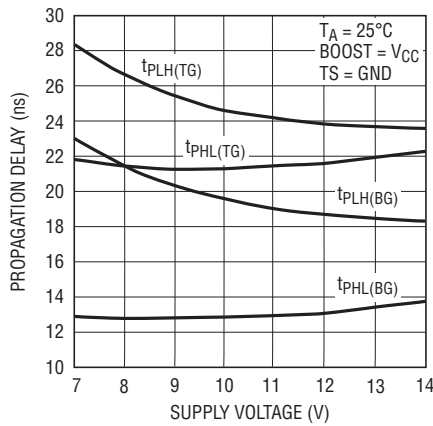
4446 G14

**Output Driver Pull-Down Resistance vs Temperature**



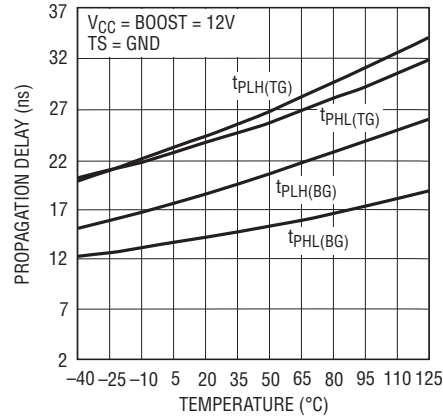
4446 G15

**Propagation Delay vs VCC Supply Voltage**



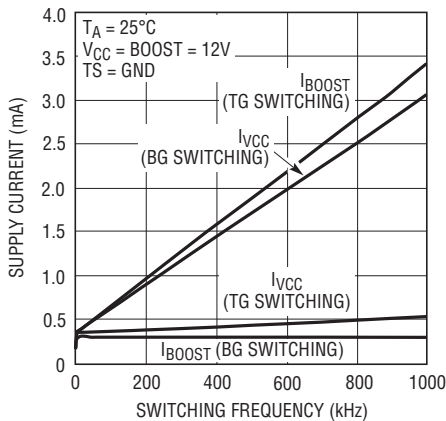
4444 G16

**Propagation Delay vs Temperature**



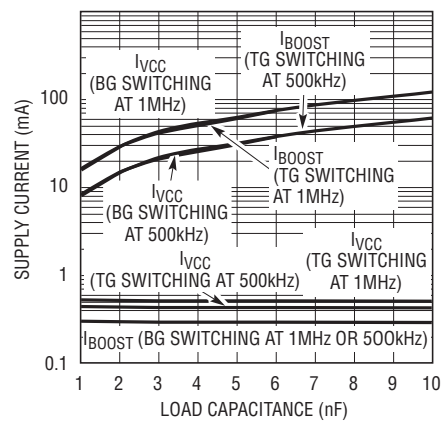
4446 G17

**Switching Supply Current vs Input Frequency**



4446 G18

**Switching Supply Current vs Load Capacitance**



4446 G19

## PIN FUNCTIONS

**TINP (Pin 1):** High Side Input Signal. Input referenced to GND. This input controls the high side driver output (TG).

**BINP (Pin 2):** Low Side Input Signal. This input controls the low side driver output (BG).

**V<sub>CC</sub> (Pin 3):** Supply. This pin powers input buffers, logic and the low side gate driver output directly and the high side gate driver output through an external diode connected between this pin and BOOST (Pin 6). A low ESR ceramic bypass capacitor should be tied between this pin and GND (Pin 9).

**BG (Pin 4):** Low Side Gate Driver Output (Bottom Gate). This pin swings between V<sub>CC</sub> and GND.

**NC (Pin 5):** No Connect. No connection required.

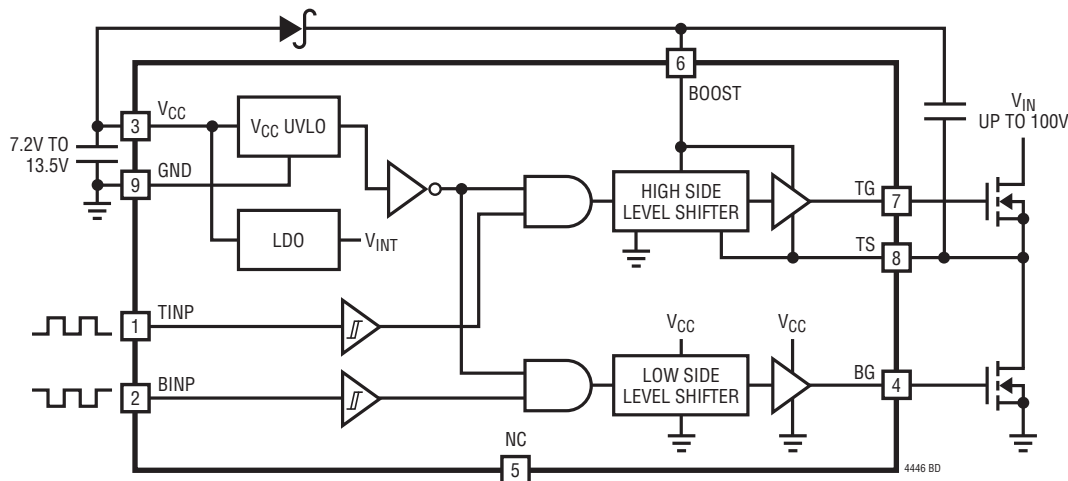
**BOOST (Pin 6):** High Side Bootstrapped Supply. An external capacitor should be tied between this pin and TS (Pin 8). Normally, a bootstrap diode is connected between V<sub>CC</sub> (Pin 3) and this pin. Voltage swing at this pin is from V<sub>CC</sub> - V<sub>D</sub> to V<sub>IN</sub> + V<sub>CC</sub> - V<sub>D</sub>, where V<sub>D</sub> is the forward voltage drop of the bootstrap diode.

**TG (Pin 7):** High Side Gate Driver Output (Top Gate). This pin swings between TS and BOOST.

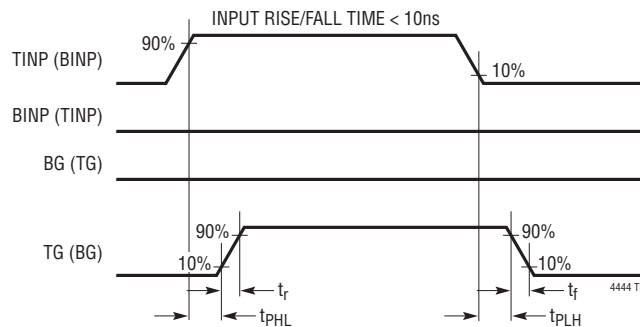
**TS (Pin 8):** High Side MOSFET Source Connection (Top Source).

**Exposed Pad (Pin 9):** Ground. Must be soldered to PCB ground for optimal thermal performance.

## BLOCK DIAGRAM



## TIMING DIAGRAM



## OPERATION

### Overview

The LTC4446 receives ground-referenced, low voltage digital input signals to drive two N-channel power MOSFETs in a synchronous buck power supply configuration. The gate of the low side MOSFET is driven either to  $V_{CC}$  or GND, depending on the state of the input. Similarly, the gate of the high side MOSFET is driven to either BOOST or TS by a supply bootstrapped off of the switching node (TS).

### Input Stage

The LTC4446 employs CMOS compatible input thresholds that allow a low voltage digital signal to drive standard power MOSFETs. The LTC4446 contains an internal voltage regulator that biases both input buffers for high side and low side inputs, allowing the input thresholds ( $V_{IH} = 2.75V$ ,  $V_{IL} = 2.3V$ ) to be independent of variations in  $V_{CC}$ . The 450mV hysteresis between  $V_{IH}$  and  $V_{IL}$  eliminates false triggering due to noise during switching transitions. However, care should be taken to keep both input pins (TINP and BINP) from any noise pickup, especially in high frequency, high voltage applications. The LTC4446 input buffers have high input impedance and draw negligible input current, simplifying the drive circuitry required for the inputs.

### Output Stage

A simplified version of the LTC4446's output stage is shown in Figure 1. The pull-up devices on the BG and TG outputs are NPN bipolar junction transistors (Q1 and Q2). The BG and TG outputs are pulled up to within an NPN  $V_{BE}$  (~0.7V) of their positive rails ( $V_{CC}$  and BOOST, respectively). Both BG and TG have N-channel MOSFET pull-down devices (M1 and M2) which pull BG and TG down to their negative rails, GND and TS. The large voltage swing of the BG and TG output pins is important in driving external power MOSFETs, whose  $R_{DS(ON)}$  is inversely proportional to the gate overdrive voltage ( $V_{GS} - V_{TH}$ ).

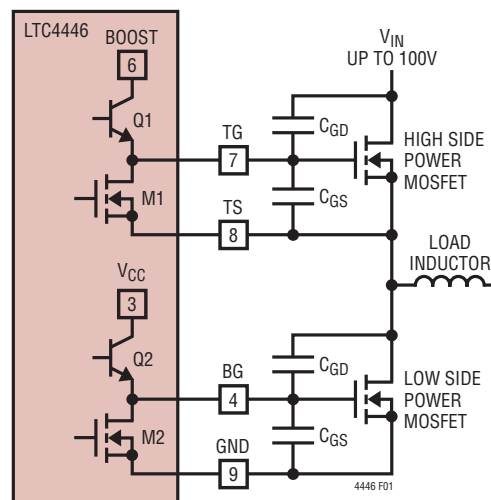


Figure 1. Capacitance Seen by BG and TG During Switching

### Rise/Fall Time

The LTC4446's rise and fall times are determined by the peak current capabilities of Q1 and M1. The predriver that drives Q1 and M1 uses a nonoverlapping transition scheme to minimize cross-conduction currents. M1 is fully turned off before Q1 is turned on and vice versa.

Since the power MOSFET generally accounts for the majority of the power loss in a converter, it is important to quickly turn it on or off, thereby minimizing the transition time in its linear region. An additional benefit of a strong pull-down on the driver outputs is the prevention of cross-conduction current. For example, when BG turns the low side (synchronous) power MOSFET off and TG turns the high side power MOSFET on, the voltage on the TS pin will rise to  $V_{IN}$  very rapidly. This high frequency positive voltage transient will couple through the  $C_{GD}$  capacitance of the low side power MOSFET to the BG pin. If there is an insufficient pull-down on the BG pin, the voltage on the BG pin can rise above the threshold voltage of the low side power MOSFET, momentarily turning it back on. With

## OPERATION

both the high side and low side MOSFETs conducting, significant cross-conduction current will flow through the MOSFETs from  $V_{IN}$  to ground and will cause substantial power loss. A similar effect occurs on TG due to the  $C_{GS}$  and  $C_{GD}$  capacitances of the high side MOSFET.

The powerful output driver of the LTC4446 reduces the switching losses of the power MOSFET, which increase with transition time. The LTC4446's high side driver is capable of driving a 1nF load with 8ns rise and 5ns fall times using a bootstrapped supply voltage  $V_{BOOST-TS}$  of 12V while its low side driver is capable of driving a 1nF

load with 6ns rise and 3ns fall times using a supply voltage  $V_{CC}$  of 12V.

### Undervoltage Lockout (UVLO)

The LTC4446 contains an undervoltage lockout detector that monitors  $V_{CC}$  supply. When  $V_{CC}$  falls below 6.15V, the output pins BG and TG are pulled down to GND and TS, respectively. This turns off both external MOSFETs. When  $V_{CC}$  has adequate supply voltage, normal operation will resume.

## APPLICATIONS INFORMATION

### Power Dissipation

To ensure proper operation and long-term reliability, the LTC4446 must not operate beyond its maximum temperature rating. Package junction temperature can be calculated by:

$$T_J = T_A + P_D (\theta_{JA})$$

where:

$T_J$  = Junction temperature

$T_A$  = Ambient temperature

$P_D$  = Power dissipation

$\theta_{JA}$  = Junction-to-ambient thermal resistance

Power dissipation consists of standby and switching power losses:

$$P_D = P_{DC} + P_{AC} + P_{QG}$$

where:

$P_{DC}$  = Quiescent power loss

$P_{AC}$  = Internal switching loss at input frequency,  $f_{IN}$

$P_{QG}$  = Loss due turning on and off the external MOSFET with gate charge QG at frequency  $f_{IN}$

The LTC4446 consumes very little quiescent current. The DC power loss at  $V_{CC} = 12V$  and  $V_{BOOST-TS} = 12V$  is only  $(350\mu A)(12V) = 4.2mW$ .

At a particular switching frequency, the internal power loss increases due to both AC currents required to charge and discharge internal node capacitances and cross-conduction currents in the internal logic gates. The sum of the quiescent current and internal switching current with no load are shown in the Typical Performance Characteristics plot of Switching Supply Current vs Input Frequency.

The gate charge losses are primarily due to the large AC currents required to charge and discharge the capacitance of the external MOSFETs during switching. For identical pure capacitive loads  $C_{LOAD}$  on TG and BG at switching frequency  $f_{IN}$ , the load losses would be:

$$P_{CLOAD} = (C_{LOAD})(f)[(V_{BOOST-TS})^2 + (V_{CC})^2]$$

In a typical synchronous buck configuration,  $V_{BOOST-TS}$  is equal to  $V_{CC} - V_D$ , where  $V_D$  is the forward voltage drop across the diode between  $V_{CC}$  and BOOST. If this drop is small relative to  $V_{CC}$ , the load losses can be approximated as:

$$P_{CLOAD} = 2(C_{LOAD})(f_{IN})(V_{CC})^2$$



## APPLICATIONS INFORMATION

Unlike a pure capacitive load, a power MOSFET's gate capacitance seen by the driver output varies with its  $V_{GS}$  voltage level during switching. A MOSFET's capacitive load power dissipation can be calculated using its gate charge,  $Q_G$ . The  $Q_G$  value corresponding to the MOSFET's  $V_{GS}$  value ( $V_{CC}$  in this case) can be readily obtained from the manufacturer's  $Q_G$  vs  $V_{GS}$  curves. For identical MOSFETs on TG and BG:

$$P_{QG} = 2(V_{CC})(Q_G)(f_{IN})$$

To avoid damage due to power dissipation, the LTC4446 includes a temperature monitor that will pull BG and TG low if the junction temperature rises above 160°C. Normal operation will resume when the junction temperature cools to less than 135°C.

### Bypassing and Grounding

The LTC4446 requires proper bypassing on the  $V_{CC}$  and  $V_{BOOST-TS}$  supplies due to its high speed switching (nanoseconds) and large AC currents (Amperes). Careless component placement and PCB trace routing may cause excessive ringing.

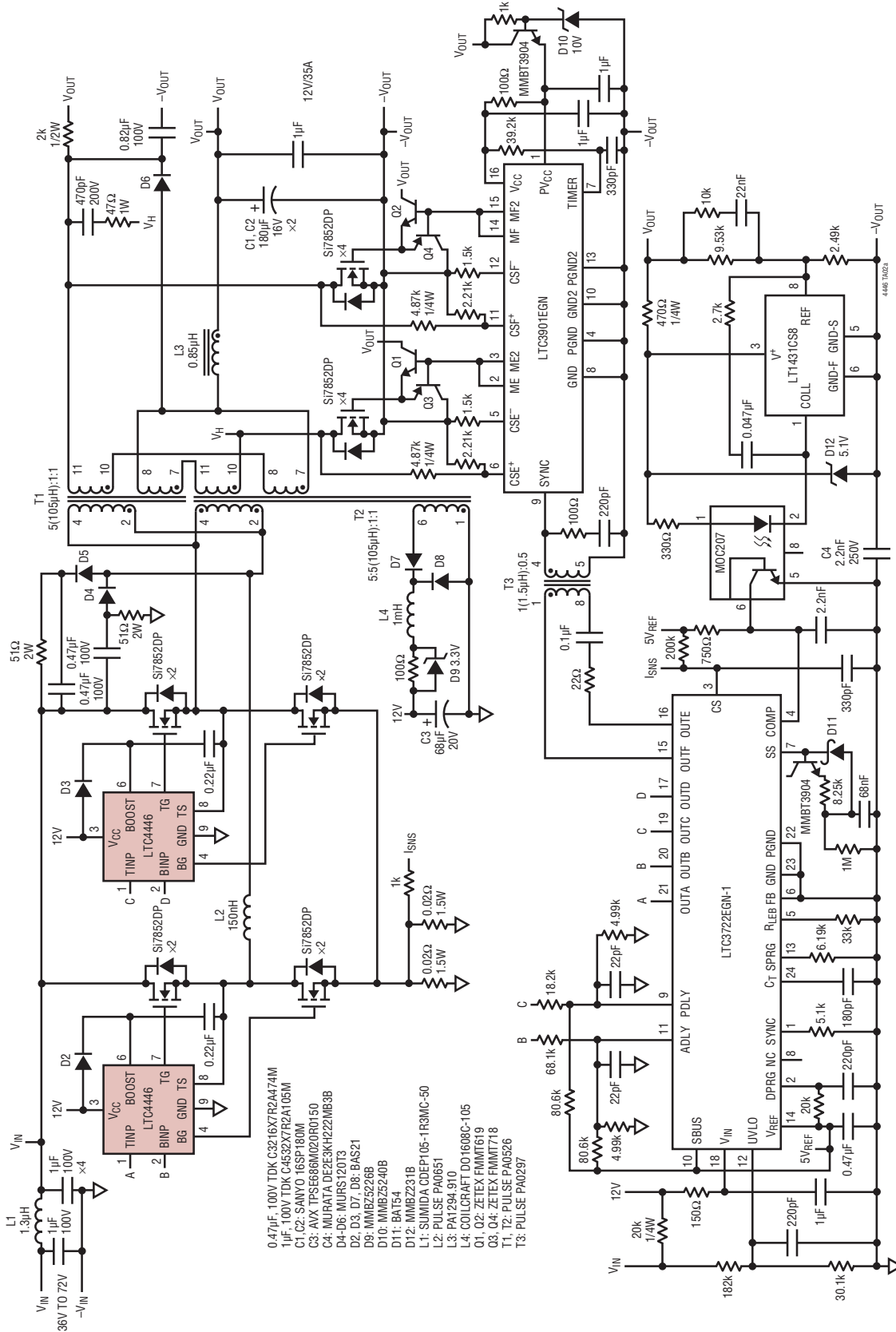
To obtain the optimum performance from the LTC4446:

A. Mount the bypass capacitors as close as possible between the  $V_{CC}$  and GND pins and the BOOST and TS pins. The leads should be shortened as much as possible to reduce lead inductance.

- B. Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LTC4446 switches greater than 3A peak currents and any significant ground drop will degrade signal integrity.
- C. Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.
- D. Keep the copper trace between the driver output pin and the load short and wide.
- E. Be sure to solder the Exposed Pad on the back side of the LTC4446 package to the board. Correctly soldered to a 2500mm<sup>2</sup> doublesided 1oz copper board, the LTC4446 has a thermal resistance of approximately 40°C/W for the MS8E package. Failure to make good thermal contact between the exposed back side and the copper board will result in thermal resistances far greater than 40°C/W.

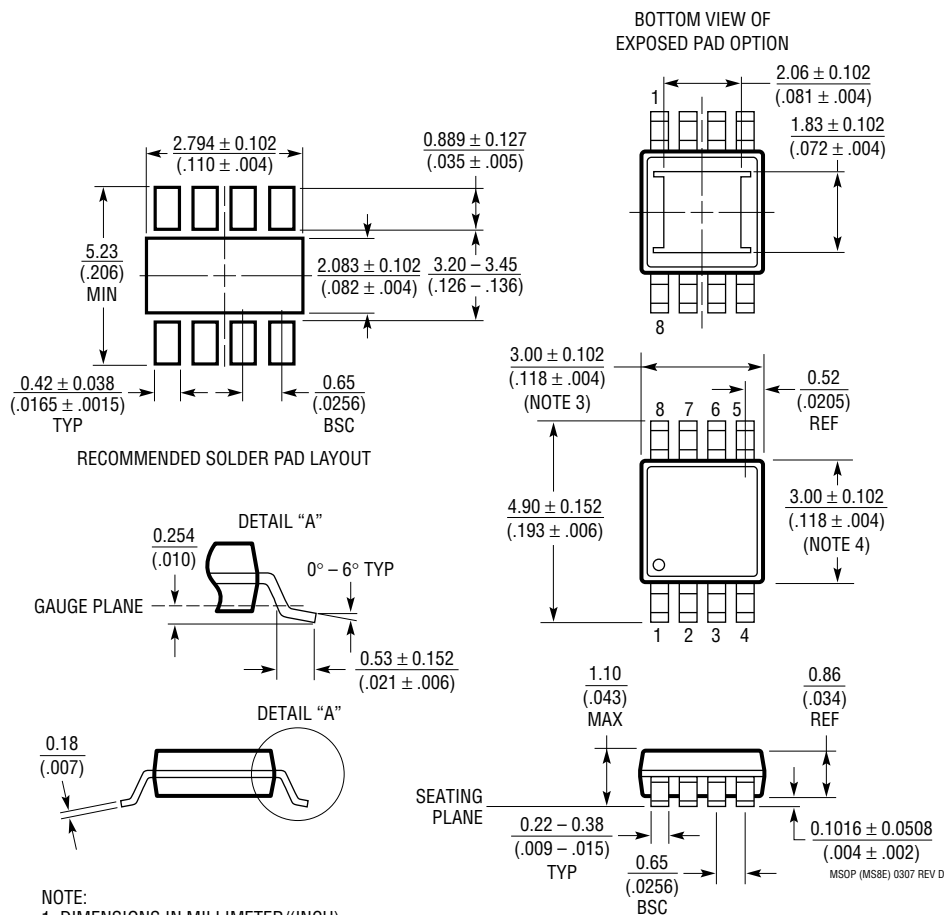
TYPICAL APPLICATION

LTC3722/LTC4446 420W 36V-72V<sub>IN</sub> to 12V/35A Isolated Full-Bridge Supply



## PACKAGE DESCRIPTION

**MS8E Package**  
**8-Lead Plastic MSOP, Exposed Die Pad**  
 (Reference LTC DWG # 05-08-1662 Rev D)



## NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

